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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,844	12/31/2001	Paras Shah	H052617.1139US0	9675

7590 07/22/2005

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EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 07/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,844	SHAH ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *5/13/05* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant states that the paragraph 0024 is amended in responding to Examiner's objection over the claim 31's subject matter (Remark, page 13, 3rd paragraph). Examiner is not able to locate any objection over the claim 31 in the prosecution history.

The amendment filed 5/13/05 regarding paragraph 0024 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The amended material is not supported by the original disclosure.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4 are rejected under 35 U.S.C. 102(a) as being anticipated by Hausauer (U.S. Patent No. 6,138,192)

Referring to claim 1: Hausauer discloses a child link (figure 1, link between structures 18 and 20), and Hausauer's physical wire to establish the child link (the PCI connections) is the

transaction identifier communication link, and each PCI transaction ID is the transaction identifier. Hausauer further discloses a plurality of transaction order queues (column 4, lines 29-31). Hausauer discloses sets of buffers/queue blocks for each PCI device pair transacting via the bridge and each pair of PCI devices only uses one particular buffer/queue block (column 4, lines 30-42). Since each pair of PCI devices only deals with one particular queue block/buffer, Hausauer discloses that each of the plurality of transaction identifiers is uniquely associated with only one of the plurality of transaction order queues. Hence, claim is anticipated by Hausauer.

Referring to claim 2: Hausauer's transaction identifier communication link comprises the child link.

Referring to claim 3: Hausauer discloses the transaction buffer (figure 5).

Referring to claim 4: Hausauer discloses a plurality of buffers (column 4, lines 29-31).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 12-13 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Hausauer and "PCI-to-PCI Bridge Architecture Specification" by PCISIG.

Referring to claim 12: Hausauer discloses a child link (figure 1, link between structures 18 and 20), and Hausauer's physical wire to establish the child link (the PCI connections) is the transaction identifier communication link. Hausauer discloses queues for storing a plurality of transactions (column 4, lines 29-52); the indexing/sorting means to track each transaction and to maintain its transaction ordering in the queue is equivalent to the transaction identifiers. Hausauer discloses a grandchild link (figure 1, link among structures 20, 22, 24, and 26), but Hausauer does not disclose a plurality of grandchild links. Hausauer's bus is a PCI bus (figure 1, structures 16 and 19) and Hausauer's bridge is a PCI-to-PCI bridge (figure 1, structure 20); thus, Hausauer's invention is constructed under the PCI standard. Furthermore, Hausauer discloses sets of buffers/queue blocks for each PCI device pair transacting via the bridge and each pair of PCI devices only uses one particular buffer/queue block (column 4, lines 30-42). Since each pair of PCI devices only deals with one particular queue block/buffer, Hausauer discloses that each of the plurality of transaction identifiers is uniquely associated with only one of the plurality of transaction order queues.

PCI specification discloses a multi-bridge architecture (page 12), and a plurality of grandchild links (page 12, links between bridge 1 and bridges 2). The PCI specification teaches one to expand the peripheral connections with the multi-bridge architecture. Hence, it would have been obvious to one having ordinary skill in the computer art to adopt the multi-

bridge/multi-link architecture onto Hausauer because the Hausauer constructs the invention with the PCI specification and the PCI specification explicitly discloses the application of the multi-bridge and multi-link architecture.

Referring to claim 13: The hardware physically connecting the Hausauer's bridges and buses is the claimed transaction identifier communication link, which comprises the child-link.

Referring to claim 15: The Hausauer discloses a plurality of transaction buffers (column 4, lines 29-31) for the child-link and for storing the transaction. A grandchild link is associated with a transaction identifier when the transaction is originated from or designated to a device connected via the grandchild link.

Referring to claim 16: The PCI spec discloses two separate grandchild links (page 12, figure 1-1) connecting with a plurality of devices. Thus, when each device under each grandchild link starts an upstream transaction, each one in the plurality of links is associated with at least two different transaction identifiers from two different devices attaching to it.

Referring to claim 17: The PCI spec discloses two separate grandchild links (page 12, figure 1-1) connecting with a plurality of devices. Thus, when one device under one grandchild link designates a transaction to another device under another grandchild link, the same transaction identifier is associated with both grandchild links.

Referring to claim 18: The PCI spec discloses that the grandchild-link connects to a bus (page 12, figure 1-1).

Referring to claim 19: The PCI spec discloses that the grandchild-link is connected to a bus-bridge (page 12, figure 1-1).

Referring to claim 20: The PCI spec discloses a bridge-bridge (page 12, figure 1-1).

7. Claims 1-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Hausauer.

Referring to claim 1: The prior art discloses a plurality of grandchild-links (figure 1, structures 162 and 164) for receiving a plurality of transactions; a child-link (figure 1, structure 152) for sending the plurality of transactions received by the plurality of grandchild-links; and the physical link between the level 2 bridge and the level 1 bridge is the claimed transaction identifier communication link (figure 1, structure 152) for sending a plurality of transaction identifiers associated with the plurality of transactions sent on the child-link. The admitted prior art discloses a PCI and PCI-X protocols (Application, page 2, line 4), and each PCI-X transaction has a sequence ID, which is the claimed transaction identifier. The admitted prior art does not disclose a plurality of transaction queues associated with one child-link and the admitted prior art does not discloses that each of the plurality of transactions identifiers is uniquely associated with only one of the plurality of transaction order queues.

Hausauer discloses a child link (figure 1, link between structures 18 and 20), and Hausauer's physical wire to establish the child link (the PCI connections) is the transaction identifier communication link, and each PCI transaction ID is the transaction identifier. Hausauer further discloses a plurality of transaction order queues (column 4, lines 29-31). Hausauer discloses sets of buffers/queue blocks for each PCI device pair transacting via the bridge and each pair of PCI devices only uses one particular buffer/queue block (column 4, lines 30-42). Since each pair of PCI devices only deals with one particular queue block/buffer, Hausauer discloses that each of the plurality of transaction identifiers is uniquely associated with

only one of the plurality of transaction order queues. Since Hausauer discloses a plurality of buffers/queue blocks for PCI devices transacting through the bridge, Hausauer discloses a plurality of transaction order queues associated with one child-link. Hausauer teaches that it is known to duplicate existing components, such as a transaction queue to strengthen and to improve the operating capacity.

In addition, the court has held that duplication of essential working parts of a device involves only routine skill in the art (MPEP 2144 and St. Regis Paper Co. v. Bemis Co., 193 USPQ 8). As Applicant stated, the St. Regis Paper Co. case states that each of the bags was taken as a complete unit and combined together for the known purpose of strengthening the entire bag structure (Remark, page 26, 3rd paragraph). As an analogy, the current Application's **claimed limitation** directs to multiply the existing transaction order queue, and multiplying the computer components for the purpose of strengthening and improving the entire general operation's capacity is a known practice, such as increasing the number of CPU or RAM.

Thus, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Hausauer's teaching onto the admitted prior art by duplicating the transaction order queues because both MPEP and the court have held that it only involves routine skill in the art to duplicate essential working parts.

Referring to claim 2: The hardware physically connecting the prior art's bridges and buses is the claimed transaction identifier communication link, which comprises the child-link.

Referring to claim 3: The admitted prior art discloses a transaction buffer (figure 1, structure 185) associated with the child-link.

Referring to claim 4: Hausauer discloses a plurality of buffers (column 4, lines 29-31).

Referring to claim 5: The prior art discloses a plurality of channels (figure 1, structures 162 and 164); wherein at least one channel of the plurality of channels is used to receive the plurality of transaction identifiers (transactions from bus devices, figure 1, structures 110). Furthermore, the admitted prior art discloses a PCI and PCI-X protocols (Application, page 2, line 4), and the PCI protocol designates the message bits 16 to 23 for specifying the bus.

Referring to claim 6: The prior art discloses a plurality of child-links (figure 1, structure 150 and additional high speed links). Hausauer discloses sets of buffers/queue blocks for each PCI device pair transacting via the bridge and each pair of PCI devices only uses one particular buffer/queue block (column 4, lines 30-42). Since each pair of PCI devices only deals with one particular queue block/buffer, Hausauer discloses that each of the plurality of transaction identifiers is uniquely associated with only one of the plurality of transaction order queues. Since Hausauer discloses a plurality of buffers/queue blocks for PCI devices transacting through the bridge, Hausauer discloses a plurality of transaction order queues associated with one child-link. Hausauer teaches that it is known to duplicate existing components, such as a transaction queue to strengthen and to improve the operating capacity.

Referring to claim 7: The prior art discloses a plurality of transaction buffers (figure 1, structures 180 and 182) for the child-link and for storing the transaction. The prior art discloses a one-to-one relationship between the buffer and transaction order queue (Application, page 3, line 1), and since the transaction order queue stores the identifiers, the prior art discloses matching the transaction identifier to a transaction buffer of the plurality of transaction buffers for the child link.

Referring to claim 8: The prior art discloses a one-to-one relationship between the buses and transaction order queues (Application, page 3, line 1). Hence, the means to associate one particular transaction order queue to one particular bus is equivalent to the claimed transaction order queue identifier.

Referring to claim 9: The prior art discloses a plurality of transaction buffers (figure 1, structures 180 and 182) for the child-link and for storing the transaction. The prior art discloses a one-to-one relationship between the buffer and transaction order queue (Application, page 3, line 1), and since the transaction order queue stores the identifiers, the prior art discloses matching the transaction identifier to a transaction buffer of the plurality of transaction buffers for the child link. The prior art discloses that the transaction queue stores identifiers for certain transactions to ensure ordering rules (Application, page 2, lines 6-7), thus the routing behavior for those transactions without transaction order rule will be the default routing behavior.

Referring to claim 10: The prior art discloses bus-bridges.

Referring to claim 11: The prior art discloses a bridge-bridge.

Referring to claim 12: The prior art discloses a plurality of grandchild-links (figure 1, structures 162 and 164) for receiving a plurality of transactions; a child-link (figure 1, structure 152) for sending the plurality of transactions received by the plurality of grandchild-links; and the hardware physically connecting the level 2 bridge and the level 1 bridge is the claimed transaction identifier communication link (figure 1, structure 152) for sending a plurality of transaction identifiers associated with the plurality of transactions sent on the child-link. The admitted prior art discloses a PCI and PCI-X protocols (Application, page 2, line 4), and each PCI-X transaction has a sequence ID, which is the claimed transaction identifier. The admitted

prior art does not disclose a plurality of transaction queues associated with one child-link and the admitted prior art does not discloses that each of the plurality of transactions identifiers is uniquely associated with only one of the plurality of transaction order queues.

Hausauer discloses a child link (figure 1, link between structures 18 and 20), and Hausauer's physical wire to establish the child link (the PCI connections) is the transaction identifier communication link, and each PCI transaction ID is the transaction identifier. Hausauer further discloses a plurality of transaction order queues (column 4, lines 29-31). Hausauer discloses sets of buffers/queue blocks for each PCI device pair transacting via the bridge and each pair of PCI devices only uses one particular buffer/queue block (column 4, lines 30-42). Since each pair of PCI devices only deals with one particular queue block/buffer, Hausauer discloses that each of the plurality of transaction identifiers is uniquely associated with only one of the plurality of transaction order queues. Since Hausauer discloses a plurality of buffers/queue blocks for PCI devices transacting through the bridge, Hausauer discloses a plurality of transaction order queues associated with one child-link. Hausauer teaches that it is known to duplicate existing components, such as a transaction queue to strengthen and to improve the operating capacity.

In addition, the court has held that duplication of essential working parts of a device involves only routine skill in the art (MPEP 2144 and St. Regis Paper Co. v. Bemis Co., 193 USPQ 8). As Applicant stated, the St. Regis Paper Co. case states that each of the bags was taken as a complete unit and combined together for the known purpose of strengthening the entire bag structure (Remark, page 26, 3rd paragraph). As an analogy, the current Application's **claimed limitation** directs to multiply the existing transaction order queue, and multiplying the

computer components for the purpose of strengthening and improving the entire general operation's capacity is a known practice, such as increasing the number of CPU or RAM.

Thus, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Hausauer's teaching onto the admitted prior art by duplicating the transaction order queues because both MPEP and the court have held that it only involves routine skill in the art to duplicate essential working parts.

Referring to claim 13: The hardware physically connecting the prior art's bridges and buses is the claimed transaction identifier communication link, which comprises the child-link.

Referring to claim 14: The prior art discloses that the child-bridge has a child-link, and the child-link has at least one channel for transmitting the plurality of transaction identifier. Furthermore, the admitted prior art discloses a PCI and PCI-X protocols (Application, page 2, line 4), and each PCI protocol designates the message bits 16 to 23 for specifying the bus, which is the claimed plurality of channels.

Referring to claim 15: The prior art discloses a plurality of transaction buffers (figure 1, structures 180 and 182) for the child-link and for storing the transaction. Since the prior art discloses a one-to-one relationship between the buffer and transaction order queue (Application, page 3, line 1), and the transaction order queue stores the identifiers, therefore, the prior art discloses matching the transaction identifier to a transaction buffer of the plurality of transaction buffers for the child link.

Referring to claim 16: The prior art discloses two separate grandchild links (figure 1, structure 162 and 164) connecting with a plurality of devices (figure 1, structures 12A-F). Thus, when each device under each grandchild link starts an upstream transaction, each one in the

plurality of links is associated with at least two different transaction identifiers from two different devices attaching to it.

Referring to claim 17: The prior art discloses two separate grandchild links (figure 1, structure 162 and 164) connecting with a plurality of devices (figure 1, structures 12A-F). Thus, when one device under one grandchild link designates a transaction to another device under another grandchild link, the same transaction identifier is associated with both grandchild links.

Referring to claim 18: The prior art discloses that the grandchild-link connects to a bus (figure 1, structures 122 and 124).

Referring to claim 19: The prior art discloses that the grandchild-link is connected to a bus-bridge (figure 1, structure 139).

Referring to claim 20: The prior art discloses that the bridge-bridge is a known practice (Application, page 1, paragraph 003, line 3, figure 1, structure 149 as a bridge-bridge).

Referring to claim 21: The prior art discloses receiving a transaction on the child-link (figure 1, structure 152). The admitted prior art discloses a PCI and PCI-X protocols (Application, page 2, line 4), and each PCI-X transaction has a sequence ID, which is the claimed transaction identifier; thus, the prior art discloses receiving a transaction identifier for the transaction link. The admitted prior art further discloses matching the transaction identifier to a transaction order queue of the plurality of transaction order queues (Application, page 3, line 1, one-to-one relationship, figure 1, structures 142 and 144) for the child-link; and routing the transaction (Application, page 1, paragraph 003, lines 1-3). The admitted prior art does not disclose a plurality of transaction queues associated with one child-link and the admitted prior art

does not discloses that each of the plurality of transactions identifiers is uniquely associated with only one of the plurality of transaction order queues.

Hausauer discloses a child link (figure 1, link between structures 18 and 20), and Hausauer's physical wire to establish the child link (the PCI connections) is the transaction identifier communication link, and each PCI transaction ID is the transaction identifier. Hausauer further discloses a plurality of transaction order queues (column 4, lines 29-31). Hausauer discloses sets of buffers/queue blocks for each PCI device pair transacting via the bridge and each pair of PCI devices only uses one particular buffer/queue block (column 4, lines 30-42). Since each pair of PCI devices only deals with one particular queue block/buffer, Hausauer discloses that each of the plurality of transaction identifiers is uniquely associated with only one of the plurality of transaction order queues. Since Hausauer discloses a plurality of buffers/queue blocks for PCI devices transacting through the bridge, Hausauer discloses a plurality of transaction order queues associated with one child-link. Hausauer teaches that it is known to duplicate existing components, such as a transaction queue to strengthen and to improve the operating capacity.

In addition, the court has held that duplication of essential working parts of a device involves only routine skill in the art (MPEP 2144 and St. Regis Paper Co. v. Bemis Co., 193 USPQ 8). As Applicant stated, the St. Regis Paper Co. case states that each of the bags was taken as a complete unit and combined together for the known purpose of strengthening the entire bag structure (Remark, page 26, 3rd paragraph). As an analogy, the current Application's **claimed limitation** directs to multiply the existing transaction order queue, and multiplying the

computer components for the purpose of strengthening and improving the entire general operation's capacity is a known practice, such as increasing the number of CPU or RAM.

Thus, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Hausauer's teaching onto the admitted prior art by duplicating the transaction order queues because both MPEP and the court have held that it only involves routine skill in the art to duplicate essential working parts.

Referring to claim 22: The prior art discloses a transaction buffer for the child-link, further comprising the step of storing the transaction in the transaction buffer (figure 1, structure 180).

Referring to claim 23: The prior art discloses a plurality of transaction buffers (figure 1, structures 180 and 182) for the child-link and for storing the transaction. Since the prior art discloses a one-to-one relationship between the buffer and transaction order queue (Application, page 3, line 1), and the transaction order queue stores the identifiers, therefore, the prior art discloses matching the transaction identifier to a transaction buffer of the plurality of transaction buffers for the child link. Furthermore, since the bridge's transaction buffer stores the transaction, bridges routes messages among different buses, the prior art includes routing the transaction to the transaction buffer.

Referring to claim 24: The prior art discloses storing transaction buffer identifier (Application, page 2, line 3), which is receiving the transaction identifier on the child-link.

Referring to claim 25: Since the prior art discloses a one-to-one relationship between the bus and transaction order queue (Application, page 3, line 1), the message from the devices on

that particular bus must match with its associated transaction order queue. Since each message of the PCI/PCI-X has an unique identifier and each device only matches to its associated transaction order queue, the prior art discloses matching the transaction identifier to a transaction buffer of the plurality of transaction buffers for the child link.

Referring to claim 26: The prior art discloses receiving a transaction on the grandchild-link (figure 1, structure 162) and sending transaction to the parent bridge. The admitted prior art discloses a PCI and PCI-X protocols (Application, page 2, line 4), and each PCI-X transaction has a sequence ID, which is the claimed transaction identifier. Hence, the prior art discloses originating and sending the transaction identifier to the parent-bridge. The admitted prior art does not disclose a plurality of transaction queues associated with one child-link and the admitted prior art does not discloses that each of the plurality of transactions identifiers is uniquely associated with only one of the plurality of transaction order queues.

Hausauer discloses a child link (figure 1, link between structures 18 and 20), and Hausauer's physical wire to establish the child link (the PCI connections) is the transaction identifier communication link, and each PCI transaction ID is the transaction identifier. Hausauer further discloses a plurality of transaction order queues (column 4, lines 29-31). Hausauer discloses sets of buffers/queue blocks for each PCI device pair transacting via the bridge and each pair of PCI devices only uses one particular buffer/queue block (column 4, lines 30-42). Since each pair of PCI devices only deals with one particular queue block/buffer, Hausauer discloses that each of the plurality of transaction identifiers is uniquely associated with only one of the plurality of transaction order queues. Since Hausauer discloses a plurality of buffers/queue blocks for PCI devices transacting through the bridge, Hausauer discloses a

plurality of transaction order queues associated with one child-link. Hausauer teaches that it is known to duplicate existing components, such as a transaction queue to strengthen and to improve the operating capacity.

In addition, the court has held that duplication of essential working parts of a device involves only routine skill in the art (MPEP 2144 and St. Regis Paper Co. v. Bemis Co., 193 USPQ 8). As Applicant stated, the St. Regis Paper Co. case states that each of the bags was taken as a complete unit and combined together for the known purpose of strengthening the entire bag structure (Remark, page 26, 3rd paragraph). As an analogy, the current Application's **claimed limitation** directs to multiply the existing transaction order queue, and multiplying the computer components for the purpose of strengthening and improving the entire general operation's capacity is a known practice, such as increasing the number of CPU or RAM.

Thus, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Hausauer's teaching onto the admitted prior art by duplicating the transaction order queues because both MPEP and the court have held that it only involves routine skill in the art to duplicate essential working parts.

Referring to claim 27: The prior art discloses that the transaction identifier is sent to the parent-bridge on a child-link (figure 1, structure 152).

Referring to claim 28: The admitted prior art discloses a PCI and PCI-X protocols (Application, page 2, line 4), and each PCI-X transaction has a sequence ID, which is the claimed transaction identifier. Since the sequence is one or more transactions associated with carrying out a single logical transfer by requester, and each transaction in the same sequence

carries the same unique sequence ID, therefore, the transaction identifier/sequence ID is determined on which the transaction was received in order to complete a sequence.

Referring to claim 29: The admitted prior art discloses a PCI and PCI-X protocols (Application, page 2, line 4), and PCI protocol specifies each message to include a bus number (bits 16 to 23).

Referring to claim 30: The prior art discloses two separate grandchild links (figure 1, structure 162 and 164) connecting with a plurality of devices (figure 1, structures 12A-F). Thus, when each device under each grandchild link starts an upstream transaction, each one in the plurality of links is associated with at least two different transaction identifiers from two different devices attaching to it.

Referring to claim 31: The prior art discloses a parent-bridge (figure 1, structure 149) including a child link (figure 1, structure 152); and a plurality of transaction order queues (figure 1, structures 142 and 144) connected to the child-link; and a child-bridge (figure 1, structure 139) connected via the child-link to the parent bridge and further comprising a plurality of grandchild-links (figure 1, structures 162 and 164). The admitted prior art does not disclose a plurality of transaction queues associated with one child-link and the admitted prior art does not discloses that each of the plurality of transactions identifiers is uniquely associated with only one of the plurality of transaction order queues.

Hausauer discloses a child link (figure 1, link between structures 18 and 20), and Hausauer's physical wire to establish the child link (the PCI connections) is the transaction identifier communication link, and each PCI transaction ID is the transaction identifier. Hausauer further discloses a plurality of transaction order queues (column 4, lines 29-31).

Hausauer discloses sets of buffers/queue blocks for each PCI device pair transacting via the bridge and each pair of PCI devices only uses one particular buffer/queue block (column 4, lines 30-42). Since each pair of PCI devices only deals with one particular queue block/buffer, Hausauer discloses that each of the plurality of transaction identifiers is uniquely associated with only one of the plurality of transaction order queues. Since Hausauer discloses a plurality of buffers/queue blocks for PCI devices transacting through the bridge, Hausauer discloses a plurality of transaction order queues associated with one child-link. Hausauer teaches that it is known to duplicate existing components, such as a transaction queue to strengthen and to improve the operating capacity.

In addition, the court has held that duplication of essential working parts of a device involves only routine skill in the art (MPEP 2144 and St. Regis Paper Co. v. Bemis Co., 193 USPQ 8). As Applicant stated, the St. Regis Paper Co. case states that each of the bags was taken as a complete unit and combined together for the known purpose of strengthening the entire bag structure (Remark, page 26, 3rd paragraph). As an analogy, the current Application's **claimed limitation** directs to multiply the existing transaction order queue, and multiplying the computer components for the purpose of strengthening and improving the entire general operation's capacity is a known practice, such as increasing the number of CPU or RAM.

Thus, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Hausauer's teaching onto the admitted prior art by duplicating the transaction order queues because both MPEP and the court have held that it only involves routine skill in the art to duplicate essential working parts.

Referring to claim 32: The prior art discloses a plurality of child-links to a plurality of child-bridges (figure 1, level 1).

Referring to claim 33: The prior art discloses that the child-bridge transmits a transaction to the parent bridge (figure 1, via the structure 152). The admitted prior art discloses a PCI and PCI-X protocols (Application, page 2, line 4), and each PCI-X transaction has a sequence ID, which is the claimed transaction identifier.

Referring to claim 34: Since the prior art discloses a one-to-one relationship between the bus and transaction order queue (Application, page 3, line 1), and the transaction order queue stores the identifiers, therefore, the prior art discloses matching the transaction identifier to a transaction queue of the plurality of transaction queue.

Referring to claim 35: The admitted prior art discloses a PCI and PCI-X protocols (Application, page 2, line 4), and the PCI protocol designates the message bits 16-23 for specifying bus number; thus, the admitted prior art discloses identifying a grandchild-link of the plurality of grandchild-links.

Referring to claim 36: The prior art discloses that the bridge routes the message to its designation (Application, page 1, paragraph 0003, lines 1-3).

Referring to claim 37: The prior art discloses the transaction buffer (figure 1, structures 180 and 186).

Referring to claim 38: The prior art discloses a plurality of transaction buffers (figure 1, structures 180, 182, and 186) connected to the child-link.

Referring to claim 39: The prior art discloses a plurality of grandchild-links (figure 1, structures 162 and 164) for receiving a plurality of transactions; a child-link (figure 1, structure

152) for sending the plurality of transactions received by the plurality of grandchild-links; and the physical link between the level 2 bridge and the level 1 bridge is the claimed transaction identifier communication link (figure 1, structure 152) for sending a plurality of transaction identifiers associated with the plurality of transactions sent on the child-link. The admitted prior art discloses a PCI and PCI-X protocols (Application, page 2, line 4), and each PCI-X transaction has a sequence ID, which is the claimed transaction identifier. The admitted prior art does not disclose a plurality of transaction queues associated with one child-link and the admitted prior art does not discloses that each of the plurality of transactions identifiers is uniquely associated with only one of the plurality of transaction order queues.

Hausauer discloses a child link (figure 1, link between structures 18 and 20), and Hausauer's physical wire to establish the child link (the PCI connections) is the transaction identifier communication link, and each PCI transaction ID is the transaction identifier. Hausauer further discloses a plurality of transaction order queues (column 4, lines 29-31). Hausauer discloses sets of buffers/queue blocks for each PCI device pair transacting via the bridge and each pair of PCI devices only uses one particular buffer/queue block (column 4, lines 30-42). Since each pair of PCI devices only deals with one particular queue block/buffer, Hausauer discloses that each of the plurality of transaction identifiers is uniquely associated with only one of the plurality of transaction order queues. Since Hausauer discloses a plurality of buffers/queue blocks for PCI devices transacting through the bridge, Hausauer discloses a plurality of transaction order queues associated with one child-link. Hausauer teaches that it is known to duplicate existing components, such as a transaction queue to strengthen and to improve the operating capacity.

In addition, the court has held that duplication of essential working parts of a device involves only routine skill in the art (MPEP 2144 and St. Regis Paper Co. v. Bemis Co., 193 USPQ 8). As Applicant stated, the St. Regis Paper Co. case states that each of the bags was taken as a complete unit and combined together for the known purpose of strengthening the entire bag structure (Remark, page 26, 3rd paragraph). As an analogy, the current Application's **claimed limitation** directs to multiply the existing transaction order queue, and multiplying the computer components for the purpose of strengthening and improving the entire general operation's capacity is a known practice, such as increasing the number of CPU or RAM. Thus, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Hausauer's teaching onto the admitted prior art by duplicating the transaction order queues because both MPEP and the court have held that it only involves routine skill in the art to duplicate essential working parts.

Response to Arguments

8. Applicant alleges that Examiner objected the abstract and Applicant is unclear as to the nature of the rejection (Remark, page 12, *Objection to the Specification*, last paragraph): Examiner is unable to locate any objection over the abstract in the previous Office Action dated 1/28/05.

9. In response to Applicant's argument that there is no prior art in the present Application (Remark, page 15, 2nd paragraph): As stated in the previous Office Action dated 1/28/05, according to the Application, page 1, starting from paragraph 0002, Applicant admitted an existing practice of a modern computer system; furthermore, the existence of the system and its

related structures and general operations upon which Applicant observes the existing system's deficiency (Application, page 2, 1st paragraph, last 4 lines). Also stated in the previous Office Action date 1/28/05, if Applicant is still contending that the figure 1 with regard its general structures or general operations were not known as a prior art, Applicant is required to submit evidence to establish such for Examiner to consider. Nevertheless, Applicant has amended the label of the figure 1 as "prior art".

Conclusion

10. The prior art made of recorded, from both previous Office Action and current Office Action, and not relied upon is considered pertinent to applicant's disclosure.

"PCI-X Addendum to the PCI Local Bus Specification" by PCI Special Interest Group, 1999, Rev. 1.0: The specification discloses the sequence ID for each transaction (page 39, paragraphs 1-2).

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-3628. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632 or on the central telephone number, (571) 272-2100. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from

commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Justin King
July 14, 2005

Glenn A. Auve
Primary Patent Examiner
Technology Center 2100